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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,256	09/11/2000	Alan S. Krech JR.	10001846-1	5584

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EXAMINER	
SHRADER, LAWRENCE J	
ART UNIT	**PAPER NUMBER**
2124	9

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,256	KRECH ET AL.	
	Examiner	Art Unit	
	Lawrence Shrader	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4 - 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans).

In reference to claim 1, Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67). Kamiyama does not teach a first selector and a second flag selector. Vidwans teaches a set of multiplexers that select a first set of signals (flags), which in turn feed a second selector creating a single flag bit as output (Figure 6). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans in order to provide a multiple stage input selector that would produce a single branching bit as a condition for a branch to be executed.

In reference to claims 4 – 5, the rejection of claim 1 is incorporated with Vidwans disclosing the use of a two stage multiplexer (Figure 9).

3. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1, and further in view of Asakawa et al., U.S. Patent 5,408,620 (hereinafter referred to as Asakawa).

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but neither Kamiyama nor Vidwans teach a plurality of branch instruction units comprising an operator logically combining branch flags to create a branch bit. Asakawa, however, teaches multiple branch instruction units (column 2, lines 50 – 56), and a circuit for processing conditional branching instructions that uses a multiple input logical AND as an operator (column 5, line 49 to column 6, line 54; Figure 7, item 132). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further modify the combination of Kamiyama and Vidwans with the teaching of Asakawa to operate multiple branching units, and to provide an operator accepting multiple flags and logically combining in order to produce a branching bit indicating a certain condition to enhance the combination of Kamiyama and Vidwans.

In reference to claim 6, the rejection of claim 2 in incorporated and references the multiple input logical AND operator (Asakawa: Figure 7, item 132).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S.

Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1, and further in view of Runaldue et al., U.S. Patent 5,479,649 (hereinafter referred to as Runaldue).

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but neither Kamiyama nor Vidwans teaches the use of programmable registers. Runaldue teaches the use of programmable registers (column 5, lines 46 – 54). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans with programmable registers as taught by Runaldue in order to store the condition flags and supply them to the logic circuits in determination of a branch condition.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1, and further in view of Ochiai et al., U.S. Patent 4,742,466 (hereinafter referred to as Ochiai).

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (column 1, lines 25 – 30), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but neither Kamiyama nor Vidwans teaches the use of a branch address comprising a plurality of bits in a conditional branch instruction. Ochiai teaches the use of a branch address comprising a plurality of bits in a conditional branch instruction (column 3, lines 1 – 4). Therefore, it would have been obvious to one skilled in the art at the

time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans with a branch address as a plurality of bits in a conditional branch instruction as taught by Ochiai in order to provide the branch address in the case of a branch.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1, and further in view of Webb et al., U.S. Patent 6,067,617 (hereinafter referred to as Webb).

The rejection of claim 1 is incorporated, and Webb further teaches the use of a conditional branch instruction comprising a bit that allows branching on various combinations of flag settings (column 9, lines 20 – 26). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans with a conditional branch instruction bit as taught by Webb in order determine on which condition to branch.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and further in view of Asakawa et al., U.S. Patent 5,408,620 (hereinafter referred to as Asakawa) and of Webb et al., U.S. Patent 6,067,617 (hereinafter referred to as Webb).

The rejection of claim 2 is incorporated. Claim 9 is rejected for the same reason put forth in the rejection of claim 8.

In reference to claims 10 and 11, official notice is taken that a dual input, single output selector/multiplexer is well known in the art with inputs arranged in various configurations.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arkin et al., U.S. Patent 6,380,730 (hereinafter referred to as Arkin) in view of Ochiai et al., U.S. Patent 4,742,466.

"Identifying..." Arkin teaches a method wherein a conditional branch instruction is identified, a set of flags are determined and stored in a register, and conditional branches are performed based on the contents of the flag register (column 7, lines 63 – 67).

Arkin does not teach assigning a branch condition address for the conditional branch instruction. However, Ochiai teaches the branch address as part of the conditional branch instruction (column 3, lines 1 – 4). Therefore, it would have been obvious to one skilled in the art at the time the invention was made that during code interpreting one might combine the method of handling conditional branches and flags as taught by Arkin with the conditional branch instruction carrying the branch address as taught by Ochiai so that the branch instruction carries the branch address.

"Interpreting..." Official notice is taken that the method of interpreting source code comprising a plurality of program instructions is well known in the art in order to produce executable code.

Official notice is taken that the encoding and storing of the conditional branch instructions with the flag into object format is well know in the art so that specific code might be executed by the computer system when certain conditions exist.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arkin et al., U.S. Patent 6,380,730 (hereinafter referred to as Arkin) in view of Ochiai et al., U.S. Patent 4,742,466

as applied to claim 12, and further in view of White et al., U.S. Patent 5,632,023 (hereinafter referred to as White).

Arkin teaches a method wherein a conditional branch instruction is identified, a set of flags are determined and stored in a register, and conditional branches are performed based on the contents of the flag register, but neither Arkin nor Ochiai teaches the reordering of a set of flags for a conditional branch instruction. White teaches a reordering of a flag sub-group for a branching function (column 34, lines 31 – 39). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the flag and branch instruction processing of Arkin with the conditional branch instruction carrying the branch address as taught by Ochiai and further combining with the teaching of White that re-orders the set of branching flags in order to optimize the code to process more efficiently.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arkin et al., U.S. Patent 6,380,730 (hereinafter referred to as Arkin) in view of Ochiai et al., U.S. Patent 4,742,466 as applied to claim 12, and further in view of Grady et al., U.S. Patent 5,276,776 (hereinafter referred to as Grady).

Arkin teaches a method wherein a conditional branch instruction is identified, a set of flags are determined and stored in a register, and conditional branches are performed based on the contents of the flag register, but neither Arkin nor Ochiai teaches the conversion of all disjunctive operations to a conjunctive equivalent. Grady teaches a system that accepts disjunctive rules and converts them to conjunctive equivalent (column 7, lines 7 – 20). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the flag and branch instruction processing of Arkin with the conditional branch

instruction carrying the branch address as taught by Ochiai and modify it with the teaching of Grady so that logical conditions might be "ANDed" together.

11. Claims 15 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and further in view of Ochiai et al., U.S. Patnet 4,742,466 (hereinafter referred to as Ochiai).

In reference to claim 15, Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67). Kamiyama does not teach a first selector and a second flag selector. Vidwans teaches a set of multiplexers that select a first set of signals (flags), which in turn feed a second selector creating a single flag bit as output (Figure 9). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans in order to provide a multiple stage input selector that would produce a single branching bit as a condition for a branch to be executed.

Niether Kamiyama nor Vidwans teaches a compiler, but Ochiai teaches a compiler that converts source code including conditional branch instructions including an address and a flag (column 2, line63 to column 3, line 12). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the compiler as taught by Ochiai with the sequencer and branching unit as taught by Kamiyama and Vidwans in order to create the object code that is processed in the system.

In reference to claim 16, the rejection of claim 15 in incorporated. Claim 16 is rejected is rejected for the same reason put forth in the rejection of claim 14.

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and of Ochiai et al., U.S. Patnet 4,742,466 (hereinafter referred to as Ochiai) as applied to claim 15, and further in view of Prasanna, U.S. Patent 6,272,599.

Kamiyama, Vidwans, and Ochiai combine to teach a compile to process conditional branch instructions, a sequence of instructions executed as object code, and a branch unit to determine whether to take a branch or not. None teach the compiler setting bits on a certain condition. Prasanna teaches a compiler capable of selectively setting bits based on a certain condition. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine Kamiyama, Vidwans, and Ochiai so that the executable code might be executed by the sequencer and branching unit with equivalent conjuntive logic (incorporated from claim 16) based on a signal flag as further taught by Prasanna.

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and of Ochiai et al., U.S. Patnet 4,742,466 (hereinafter referred to as Ochiai) as applied to claim 15, and further in view of Akiyama, U.S. Patent 5,534,799.

Kamiyama, Vidwans, and Ochiai combine to teach a compile to process conditional branch instructions, a sequence of instructions executed as object code, and a branch unit to

determine whether to take a branch or not. None teach arithmetic logic units (ALU) that supply a plurality of flags. Akiyama teaches an ALU that supplies a plurality of flags. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use the teaching of Akiyama to further modify the combination of Kamiyama, Vidwans, and Ochiai so that the executable code might be executed by the sequencer and branching unit supplying flags appropriate to certain conditions required by the branch instruction.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 6,182,211 to Yamasaki, conditional branch control.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046. The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Lawrence Shrader
Examiner
Art Unit 2124

March 24, 2003

TUAN Q. DAM
PRIMARY EXAMINER